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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/723,592

11/26/2003

Augustus K. Uht

022193-010111US

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12/21/2004

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EXAMINER

PHU, PHUONG M

ART UNIT

PAPER NUMBER

2631

DATE MAILED: 12/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/723,592

Applicant(s)

UHT, AUGUSTUS K.

Examiner

Phuong Phu

Art Unit

2631

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 September 2004.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2-18 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☒ Claim(s) 2-11 is/are allowed.
6) ☒ Claim(s) 12-18 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 9/7 & 11/22.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the Amendment filed on 9/07/04.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 12-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada (4,288,874), newly-cited.

-Regarding to claim 12, see figures 2-4 and col. 4, line 25 to col. 7, line 9, Yamada discloses a system (see figure 2) comprising:

tracking logic (SR) representing a worst case delay path for said system logic;
signal input means (D1) providing logic operation input (SSX) to said tracking logic;
tracking logic monitor (E1, E2, E3, A1, A2) for monitoring for errors in logic operation output of said tracking logic to report faults (SA1, SA2);
a frequency controllable clock (SVCO) in a feedback loop with said tracking logic monitor; and
a servo (VCO) for slowing frequency of said clock upon said tracking logic monitor detecting an operation fault (SA1) in said tracking logic to a clock frequency at which no fault is detected (see figures 2 and 3, and col. 5, lines 10-25).

-Regarding to claim 13, in Yamada , said servo can inherently be operative to increase or decrease frequency of said clock after no fault is detected (see figures 3 and 4, and col. 5, lines 10-25, and col. 6, lines 37-45).

-Regarding to claim 14, Yamada discloses that said tracking logic includes a time delay (SR) (see figure 2) for producing an operational safety margin to guaranty that a fault occurs in the tracking logic (detected by (E1, E2, E3) before a fault can occurred (detected by (A1, A2) in the system.

-Regarding to claim 15, Yamada discloses that said signal input means is operative to produce a sequence of digital values (SD1) including alternating logic one and logic zero (see figure 3).

-Regarding to claim 16, Yamada discloses that said signal input means is operative to produce a digital bit stream (SD1) of alternating logic ones and logic zeros (see figure 3).

-Regarding to claim 17, Yamada discloses that said tracking logic monitor comprises an exclusive OR logic gate (E3) (see figure 2) for yielding a logic transition such that timing alone determines transition to a too fast state (SA1) and transition a too slow state (SA2).

-Regarding to claim 18, Yamada discloses that the tracking logic monitor further includes a flip flop (D2) (see figure 2) for controlling the frequency of the frequency controllable clock in response to output of said exclusive OR logic gate.

Allowable Subject Matter

4. Claims 2-11 are allowed.

Response to Arguments

5. Applicant's arguments filed on 9/7/04 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the ~~THREE-MONTH~~ shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuong Phu whose telephone number is 571-272-3009. The examiner can normally be reached on M-F (6:30-2:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2631

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phuong Phu

Phuong Phu
12/15/04

**PHUONG PHU
PRIMARY EXAMINER**

Phuong Phu
Primary Examiner
Art Unit 2631